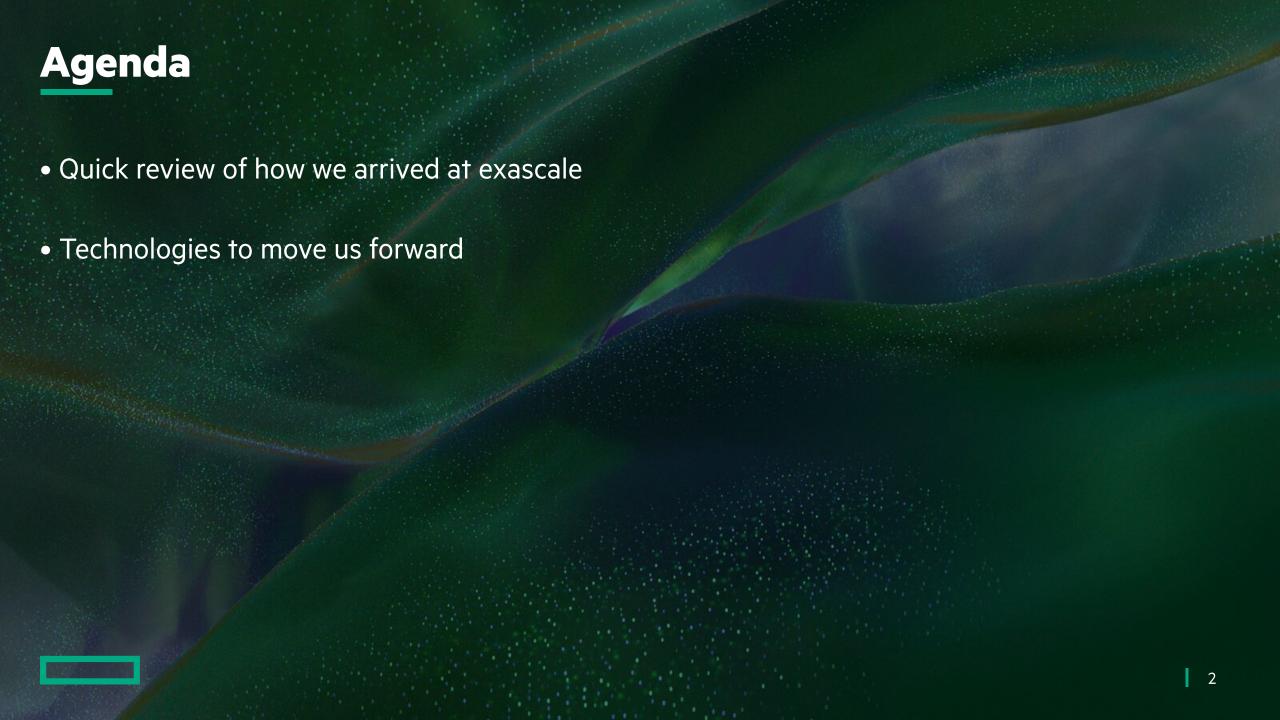


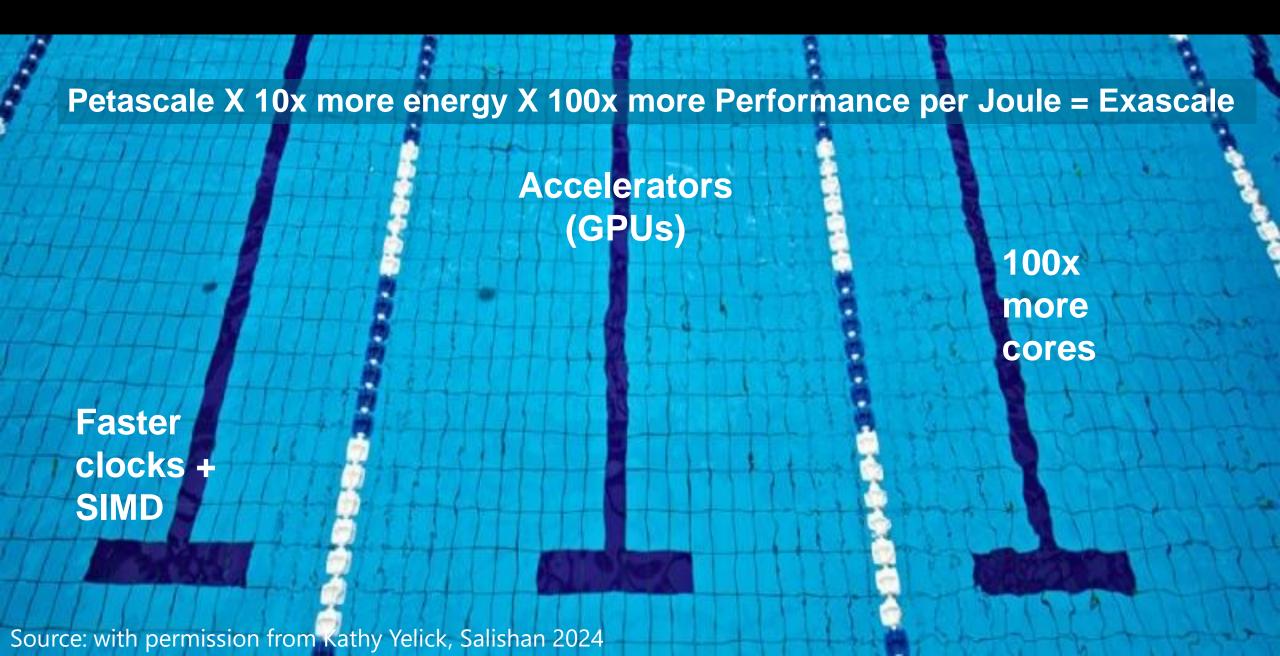
# Technologies for Future HPC and Al Systems

Dr. Robert W. Wisniewski HPE Fellow Chief Architect HPC and Al Solutions

March 18, 2025



#### Exascale Architecture Plans (2008)



# The Swim Lanes

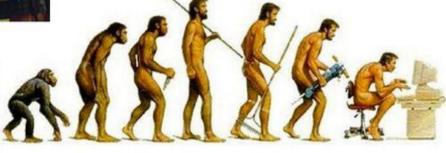
#### Obligatory Exascale Swim Lanes Slide



# **How to Get There**

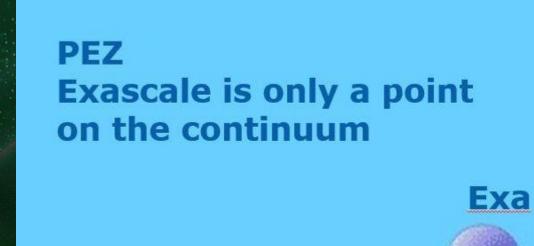
#### **Revolutionary versus Evolutionary**





• Which one ?

# PEZ – A Continuum



Zeta





Source: Wisniewski SOS 2014

#### **HPE Large-Scale HPC and AI Machines**

Helping organizations tackle the grand challenges of humankind

37,632

63,744

44,544

**GPUs** 

**GPUs** 

**APUs** 







100% liquid-cooled HPE Cray EX supercomputer

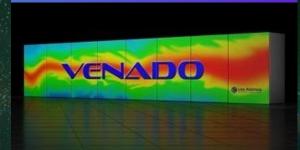
High performance GPU accelerated blades

HPE Slingshot exascale interconnect

Cray ClusterStor file systems

#### **Enabling Large-Scaling AI Workloads Around the Globe**





10 EFLOPS

single-precision AI Performance with NVIDIA GH200 superchips





**20 EFLOPS** 

single-precision AI Performance with NVIDIA GH200 superchips





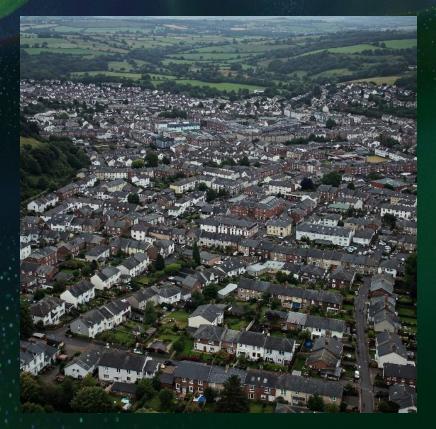
21 EFLOPS

single-precision AI Performance with NVIDIA GH200 superchips

### Power – A Little or A Lot

- Frontier 22.7 MW (https://en.wikipedia.org/wiki/Frontier\_(supercomputer))
- Aurora 38.7 MW (https://en.wikipedia.org/wiki/Aurora\_(supercomputer))

• Combined powers a small city (40K people)



#### Power - A Little or A Lot

- GPT-4 training used over 50 gigawatt-hours
  - 0.02% of the electricity California generates in a year
  - 2200 hours or 92 days on Frontier
  - 10T mode estimate 5000 gigawatt-hours
- LHC 200 MW



### Power – A Little or A Lot

- The Gigawatt Data Center Campus is Coming
- Amazon Web Services recently bought a data center co-located with a nuclear power facility, where it hopes to gradually deploy up to 960 megawatts
- https://www.datacenterfrontier.com/hyperscale/article/ /55021675/the-gigawatt-data-center-campus-iscoming



### Parallelism and Fat versus Thin Nodes

- Sequoia 20PF circa 2012, had 96 racks \*1024 nodes/rack +16 cores/node == 1,572,864 \*4 threads/core = 6,291,456 threads
- Concern was we would need 50x that number of threads

https://en.wikipedia.org/wiki/Sequoia\_(supercomputer)



#### Parallelism and Fat versus Thin Nodes

image source: Oak Ridge National Lab





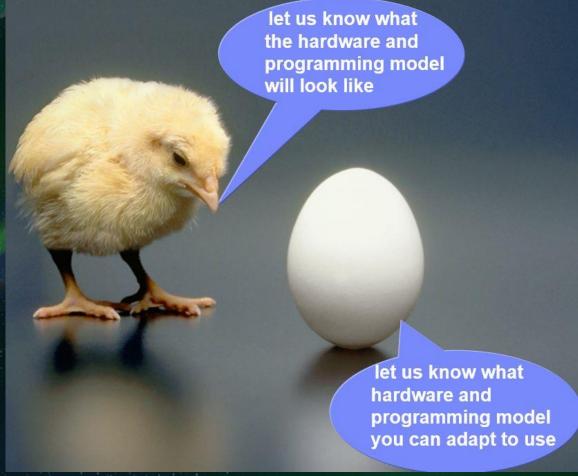
- Frontier is 74 cabinets, 128 nodes per cabinet
  - 1 AMD Epyc 7713 "Trento" CPU and 4 AMD Instinct MI250X GPUs per node
- Frontier has 9,472 CPUs \* 64 cores/CPU == 606,208 cores \* 2 threads/core == 1,212,416 threads
- Frontier has 37,888 GPUs each GPU has 2 GCD (Graphic Compute Dies) with 110 CU (Compute Units) per die == 8,335,360 cores with 64 threads (a wavefront) = 533,463,040 threads

#### Parallelism and Fat versus Thin Nodes

- Sequoia 6,291,456 threads
- Frontier
  - 1,212,416 CPU threads
  - 533,463,040 GPU threads
- The number of GPU threads exceeds what we thought thread count would be
  - The number of CPU threads is meaningfully less than predicted
  - GPU hardware and software help hide that high degree of parallelism
- Fat nodes help significantly
  - Lower surface to volume ratios reduces global communication
  - Fewer OSes put less pressure on the reliability of each instance
  - Fewer nodes ease the burden of providing scalable and reliable system management software

### Software and Programming Model

- Programming model did not substantially change
  - -Did not need all new language/runtime and model
  - -MPI + X still here
  - -Kokkos and Raja emerged and their usage broadened
  - -Kokkos also helping drive C++ standards
- Moving to GPUs was a massive effort, but primarily due to accelerator model and parallelism rather than the GPU itself
- Fat nodes relieve some of the software scalability challenges
  - Helped with reliability challenges due to absolute number of instance of software stack running
    - Has not solved hardware MTBF



Source: Wisniewski Salishan 2011

### Where We are Going: Taking Stock

- Thought we were going to do it in 20MW
  - Many people did not think so, but that was the target
- Thought it was going to take a new programming model and rewrite of all codes
  - There was a massive effort to restructure codes for GPUs
    - –Will the work that was done, at least for the codes that utilized Kokkos or Raja, carry forward
- Thought parallelism was going to swamp us
  - It grew, but we managed to [mostly] hide it with a hierarchical layer
- Thought reliability was going to require fault tolerant computing
  - We managed to eke this one out, but MTBF for capability jobs is counted in hours now
- New theme: mixed precision playing an increasing important role
- New theme: Al
- HPC has become like an aircraft carrier



Source: Al generated



Source: Al generated

### Where We Are Going: Technical Themes

- Hide complexity behind a layer
  - Threading, parallelism: small and large, programming model
- Improve performance through tighter coupling
  - Compute to memory, compute to compute, compute to communication
- Macro heterogeneity
  - Quantum common example, but perhaps more : Al training, Al inference, HPC
- Handle reliability
  - Enhance approach to fault tolerance, tolerate failures in the small at least
- Complex workflows
  - Spanning machines and sites
  - Spanning edge to supercomputer to cloud
  - Containing massive and secured data
- Sustainability and power

#### **Arkouda**

An open-source Python package providing interactive data analytics at supercomputing scale.

#### >>> Transform the way you work with big data

#### **EASY TO USE**

Provides an API data scientists are familiar with based on Pandas/NumPy

#### **POWERED BY CHAPEL**

Powered by a parallel distributed server written in Chapel

#### **FAST & SCALABLE**

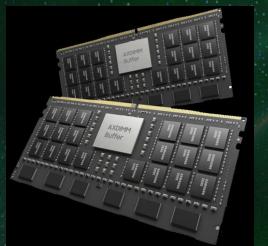
Outperforms NumPy on a single Node and has scaled up to 8,000+ Nodes

#### **EXTENSIBLE & CUSTOMIZABLE**

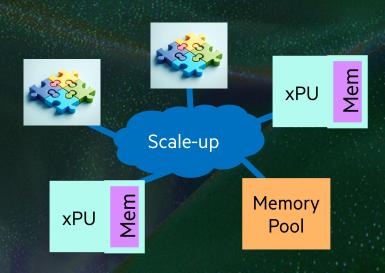
Extend Arkouda's capabilities by creating specialized functions

### **Tight Coupling**

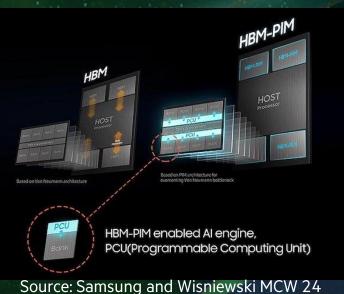
Samsung AXDIMM



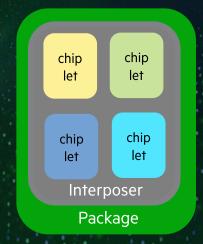
Source: Samsung and Wisniewski MCW 24



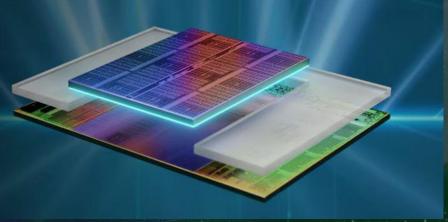
Source: Al generated



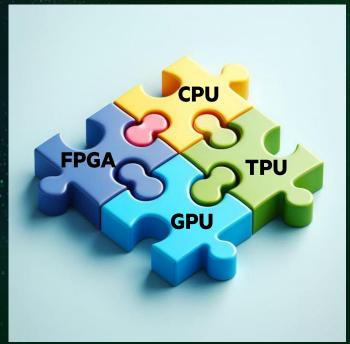
Compute to memory
Compute to compute
Compute to communication



AMD V-Cache



https://www.amd.com/en/products/processors/ technologies/3d-v-cache.html



Source: Al generated

#### **Quantum Computing Integration at HPE**

#### Integrating classical and quantum systems

to harness diverse accelerators that maximize run-time, efficiency, sustainability, and security

### Unified workflow environment

#### Simplify the end user experience

Software framework to harness accelerators most suitable for each segment of a workflow

### Large-scale quantum simulation

#### **Toward industrial scale**

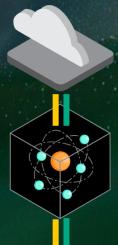
HPC systems used to simulate and test quantum advancements

### Quantum-inspired accelerators

#### Solve intractable problems

Non-conventional acceleration of algorithms explored by the quantum computing community

## Integration of quantum accelerators





Hewlett Packard **Labs** 



HPE HPC & Al Business Group



#### **Innovation partners**

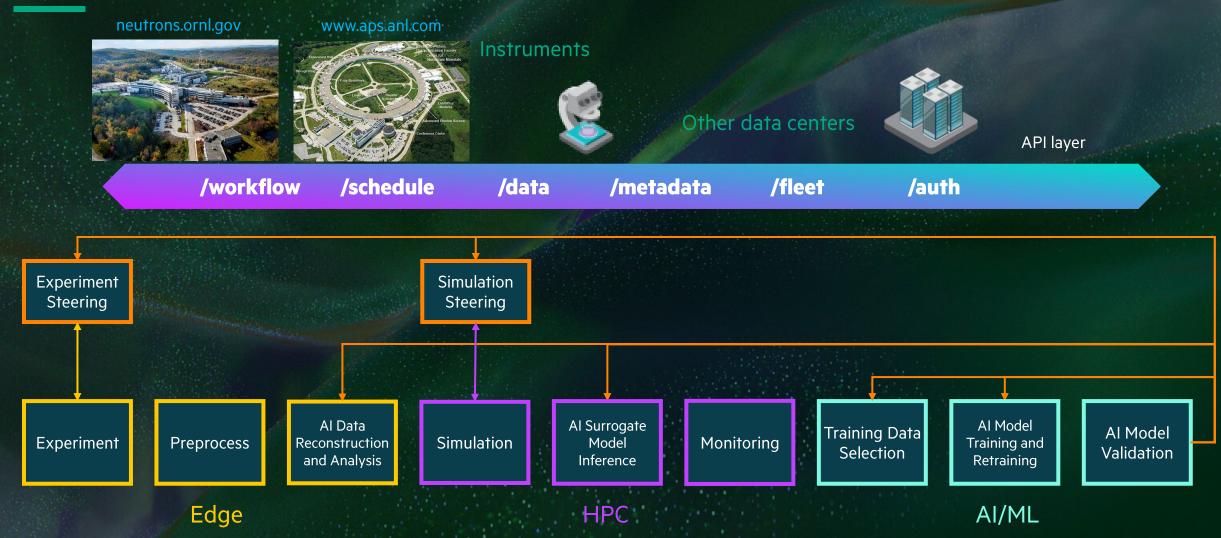
(academic, industrial, government)

Heterogenous computing development

Quantum computing development

### Common Federation Framework: Workflow Deployment SDK

Enables Federated Hybrid Workflows on Data from Edge to Extreme Scale to Cloud

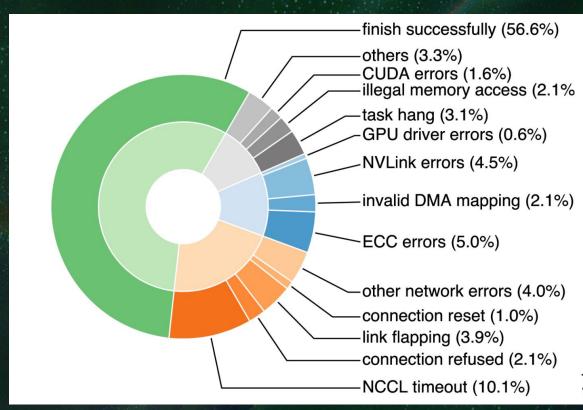


### **Al Strategy**

- HPE delivers the most HPC computing on the top 500
  - HPE sells over 2x the amount of dedicated AI computing as HPC computing
- Driving to make common AI frameworks work out of the box on our systems
  - Working to address networking, compiler, development, etc. issues
- We will leverage our expertise to augment and enhance AI systems
  - Provide tools and capability to scale AI and get it to be reliable
  - Provide frameworks to connect HPC to Al
  - Provide tools to build and deploy federated AI workflows

### What Happens at Scale

• As leadership-class AI workloads have grown, concerns about reliability have increased



Component	Category	Interruption Count	% of Interruptions	
Faulty GPU	GPU	148		
GPU HBM3 Memory	GPU	72	17.2%	
Software Bug	Dependency	Dependency 54		
Network Switch/Cable	Network 35		8.4%	
Host Maintenance	Unplanned Maintenance	32	7.6%	
GPU SRAM Memory	GPU 19		4.5%	
GPU System Processor	GPU	17	4.1%	
NIC	$\operatorname{Host}$	7	1.7%	
NCCL Watchdog Timeouts	Unknown	7	1.7%	
Silent Data Corruption	GPU	6	1.4%	
GPU Thermal Interface + Sensor	GPU	6	1.4%	
SSD	$\operatorname{Host}$	3	0.7%	
Power Supply	Host	3	0.7%	
Server Chassis	$\operatorname{Host}$	2	0.5%	
IO Expansion Board	Host	2	0.5%	
Dependency	Dependency	2	0.5%	
CPU	Host	2	0.5%	
System Memory	Host	2	0.5%	

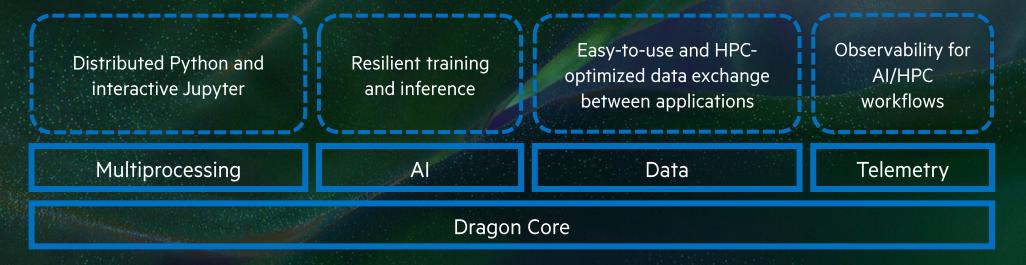
Table 5 Root-cause categorization of unexpected interruptions during a 54-day period of Llama 3 405B pre-training. About 78% of unexpected interruptions were attributed to confirmed or suspected hardware issues.

https://arxiv.org/pdf/2401.00134

https://arxiv.org/pdf/2407.21783

### Coupling AI and HPC

Dragon is a composable distributed runtime that enables users to create sophisticated, scalable, resilient, and highperformance AI/HPC applications, workflows, and services through standard Python interfaces.



- 2 100X faster data processing than Ray
- Scalable to over 1000 nodes
- Multi-system features offer a hybrid experience, spanning from laptop to supercomputers

- Open-source or HPE-optimized packages
- Well-documented with numerous cookbook examples and easy setup

https://developer.hpe.com/platform/dragonhpc/home/ https://github.com/DragonHPC/dragon

### Holistic Power and energy Management (HPM)

Concept: System Administrator and/or User define optimization policy

Minimum resources

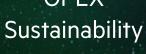
**Maximum performance** 

#### Holistic power and energy management tools

HPE's automatic workload control delivers desired outcome

#### **Possible constraints**

Power Cooling OPEX



#### **Monitoring**

- Data
- Events
- Decisions

- Dynamically balance between available power/cooling, optimized resource usage, and workload performance
- Balance facility efficiency and system operation with minimal performance impact

<sup>\*</sup> Potentially up to 50+% power and TCO savings

# A TCO Savings Example

Estimates for 8 theoretical racks (each 200kW IT nameplate power)	No Management	Uniform Static	Strategy 1	Combine (Strategy 1&2)	Combine (Strategy 1&2)
Application Performance	100%	>90%	>99.1%	>95%	>90%
IT compute power (MW)	1.6	1.2	1.2	0.9	0.7
Facility Power procured (MW)	2.3	1.7	1.7	1.2	1.0
OPEX 5 years (Million US)	>=8.4	8.4	8.4	6.0	5.0
CAPEX savings (Million US)	0.0	4.3	4.3	7.5	9.3
OPEX savings over 5 years(Million US)	0.0	0.0	0.0	2.4	3.4
Potential annual OPEX savings (Million US)	0.0	0.0	0.0	0.5	0.7
Perf/procured Watt efficiency (relative)	1.00	1.23	1.35	1.79	2.14

### Racks

- Publicly vendors have stated chip powers through 1200W
  - https://www.theregister.com/2024/03/18/nvidia\_turns\_up\_the\_ai/
  - Likely to increase 2x
  - Keeping current density drives significant rack power and cooling challenges









Cooling efficiency and capacity (kW/rack) increases from left to right

#### Leadership Class Performance

- The fastest and most capable HPC/AI solutions are ready for the future, with cutting-edge chip technology, advanced workload software and the latest in high-speed fabric
- Open Standards
  - An open rack framework with industry standard OCP motherboards decrease time to market while being adaptable with rapidly changing HPC and emerging Al-focused architectures
- Revolutionary Cooling
  - Innovative power management and cooling infrastructure enables customers to match workload needs and sustainability goals with warm facility water

#### The Future of Sustainable Data Centers

