# arm

# Unlocking Custom Silicon Through Chiplet Standards Ecosystem

SOS27

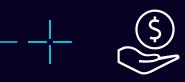
Joshua Randall, Arm March 18, 2025

# Unique Pressures are Facing the Industry



#### **Time to Market Demands**

Design talent is needed, alongside the need for performance and validation





#### **Advanced Node Cost**

Costs continue to rise



#### **Need for Specialized Silicon**

Moore's Law is slowing down, data concerns are growing, and sustainability is increasingly important



# Chiplets Offer New Opportunity



Lower design costs, higher yield, fewer defects, and better scalability

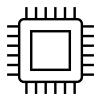


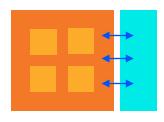
Customization, flexibility, composability, and faster design turn-around time

...requires standardization



# Changing the approach to system design









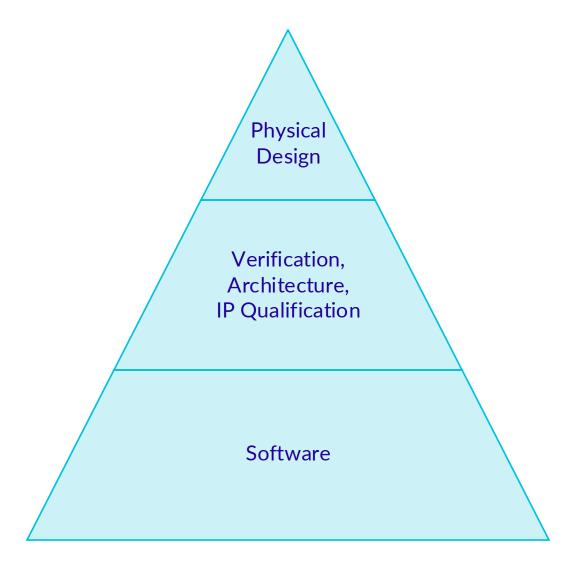
Prior: Off-shelf silicon Limited set of options to do acceleration on PCB or in system

Today: Custom SoC's using IP that integrates acceleration chiplets

Beyond: Ecosystem of interoperable and reusable chiplets

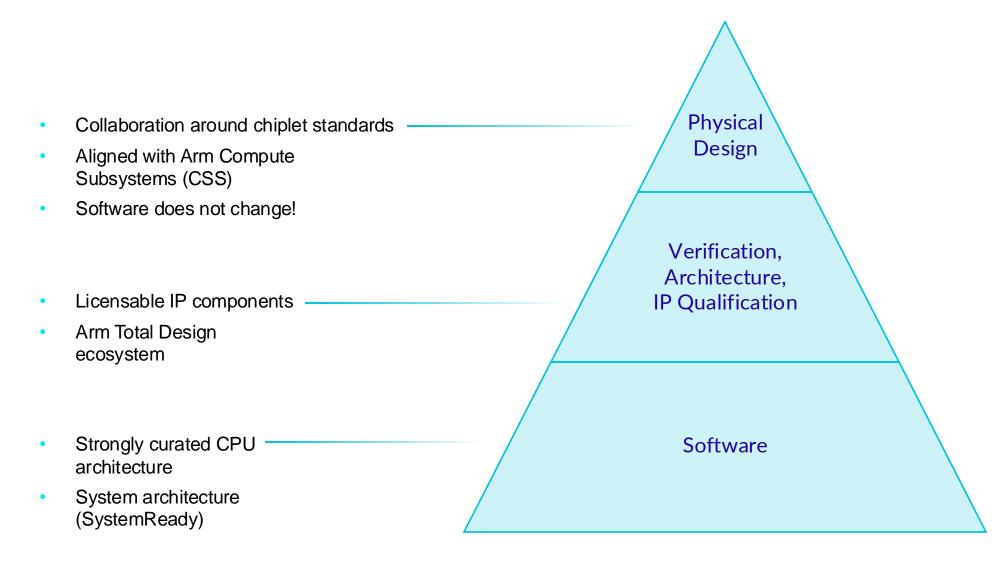


# Reality Check: The Costs of Custom Silicon



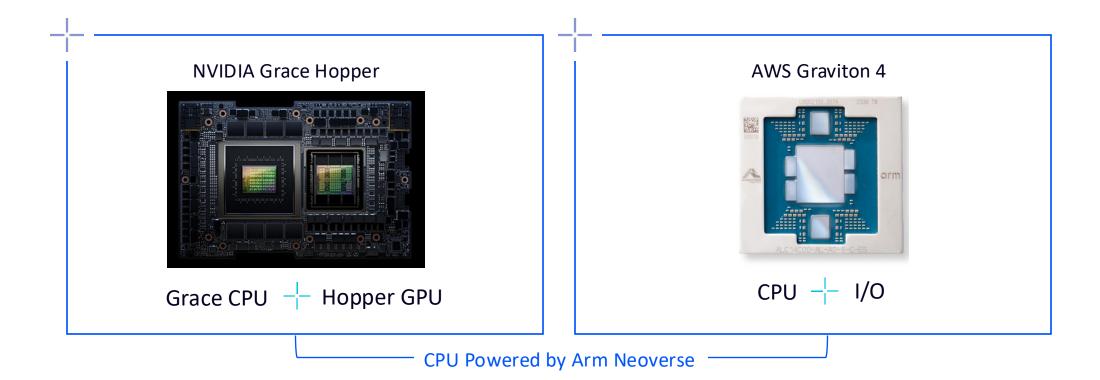


## Chiplet Standards Depend on a Strong Foundation





# Leading Cloud & Al SoCs Use Chiplets Today



#### The Road to an Open Chiplet Marketplace

# INCREASE REUSABILITY

INCREASE FLEXIBILITY AND PERFORMANCE

#### Single vendor

Proprietary chiplets

#### **Semi-custom chiplet** ecosystem

- Multi-vendor
- Protocol, transport & PHY standardization required for interoperability

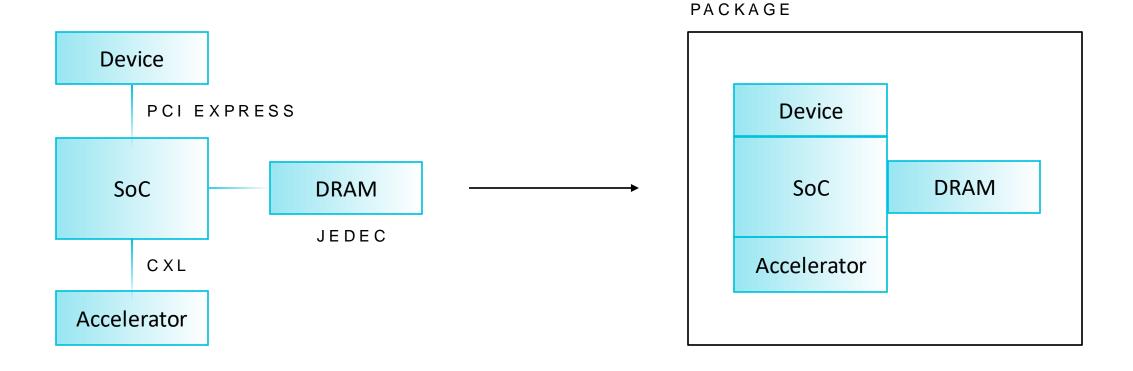
We are here!

#### Multi-vendor chiplet marketplace

- Silicon qualification & reliability
- Profiles & capabilities
- Pre/post-silicon test & debug
- Software standards
- Mechanical, thermal & power



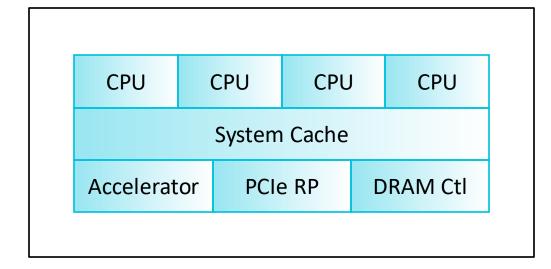
# Aggregation Across the Motherboard



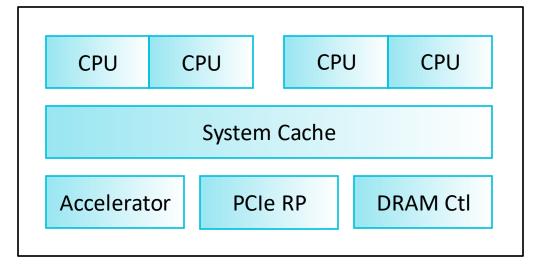


## Disaggregation of a System on Chip

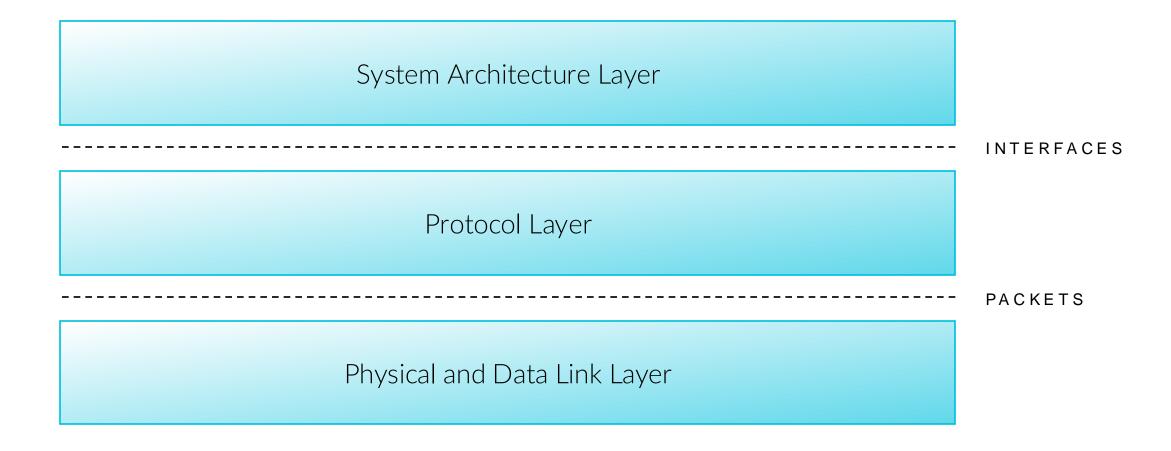
SOC



PACKAGE



#### Separate into Layers...



## Applying to System Types...

AGGREGATION ACROSS MOTHERBOARD DISAGGREGATION OF AN SOC System Architecture Layer System Architecture Layer INTERFACES Protocol Layer Protocol Layer **PACKETS** Physical and Data Link Layer

### Matching to Standards Ecosystem...

AGGREGATION ACROSS MOTHERBOARD DISAGGREGATION OF AN SOC Well-established device types: SYSTEM ARCHITECTURE Host, Endpoint... INTERFACES AMBA Existing protocols PROTOCOL PCI Express, CXL PACKETS Other standards, UCle, Universal Chiplet, PHYSICAL and proprietary Interconnect Express

#### Introducing the Chiplet System Architecture



**System Topologies** 



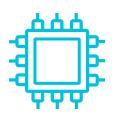
**Chiplet Types** 



**Interface Mapping** 

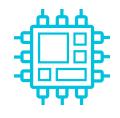
### Why AMBA?

AMBA is the standard for SoC communications underpinning silicon IP & fabless design today



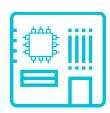
Fragment a monolithic die

into multiple chiplets



System consolidation of platform

components into chiplets



PCIe/CXL interface of choice

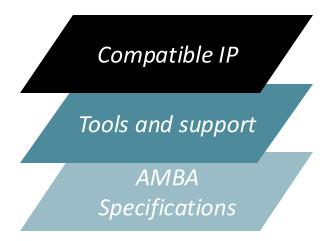
AMBA most prevalent on-die fabric

#### Widely adopted open standard

- Freely available & platform independent
- Long heritage of dependability & trust
- Billions of devices over 27+ years

#### **Common standard for a variety of designs**

- Flexibility and scalability
- Design reuse & low-friction integration
- Reduced TCO & TTM

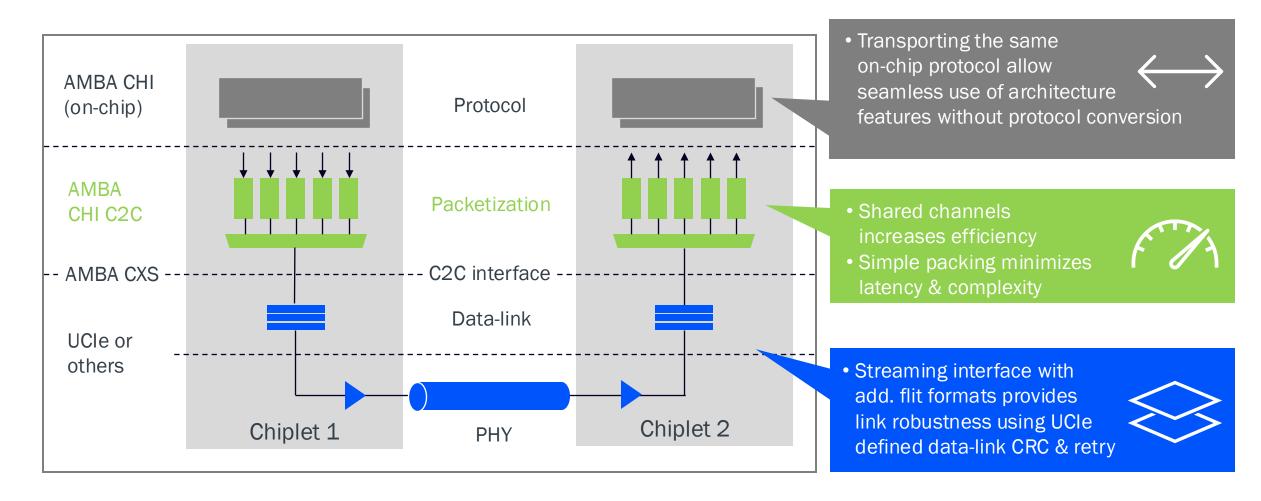


Thriving ecosystem & comprehensive marketplace



#### Chiplet-to-Chiplet Architecture

Layered architecture allows use of third-party and industry standard data-link & PHYs

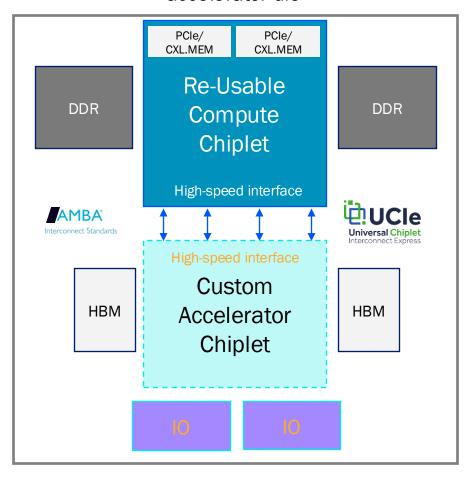


#### The Standards Stack for Chiplets

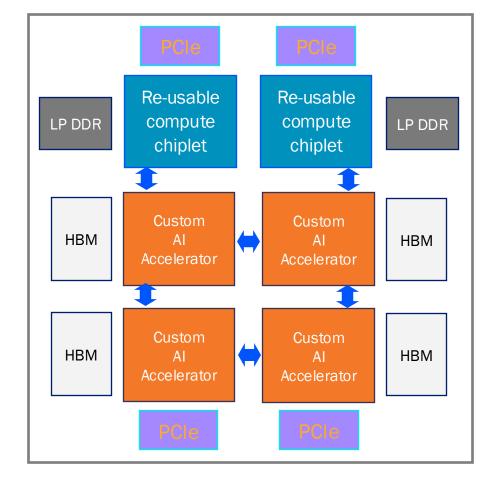
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#### Real-world Chiplet Implementation Examples

Standards-compliant compute and I/O dies, supporting attachment of market-specific accelerator die

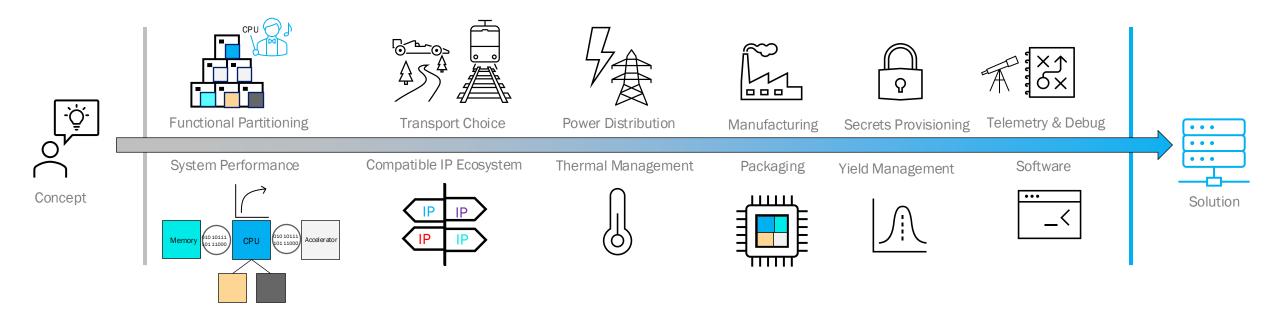


Multi-party compute and accelerator chiplet design, fabrication, and advanced packaging collaboration





### But Chiplets Introduce Challenges



#### Specifications from Industry Standards Bodies













#### Arm Total Design Partner Ecosystem

A global network of expert silicon design partners







arm

Merci Danke Gracias Grazie 谢谢 ありがとう Asante Thank You 감사합니다 धन्यवाद Kiitos

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